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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

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| LIU, LI |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/589,349 | ABE ET AL. | |
| | Examiner | Art Unit | |
| | LI LIU | 2613 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *12-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/11/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Information Disclosure Statement*

1. The information disclosure statement (IDS) submitted on 8/11/2006 is being considered by the examiner.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 12, 16, 18 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Ito et al (US 2001/0015845).

1). With regard to claim 12, Ito et al discloses an optical receiver (Figure 8) comprising:

an optical divider (Figure 8, the optical divider 8) that divides an optical input signal into a plurality of paths;

a plurality of optical-to-electrical converters (the photoelectric converters 1 in Figure 8) that respectively converts the divided optical input signals into electrical signals;

a plurality of discriminators (the code decision units 3 in Figure 8) that respectively outputs discrimination results by discriminating the electrical signals output

from the optical-to-electrical converters based on predetermined thresholds ([0042] and [0043]); and

an operational circuit (the OR circuit 5 in Figure 8) that performs a predetermined logical operation with the discrimination results output from the discriminators.

2). With regard to claim 16, Ito et al discloses wherein the predetermined thresholds of the discriminators are substantially equal (Figures 5 and 6, the predetermined thresholds of the discriminators are substantially equal).

3). With regard to claim 18, Ito et al discloses wherein the operational circuit is a logical OR circuit (Figure 8, the logical OR circuit 5).

4). With regard to claim 22, Ito et al discloses an optical communication system (Figure 8, and [0002], "relates to an optical transmission system using RZ (Return to Zero)-modulated signals") comprising:

an optical transmitter that transmits an optical signal (as shown in Figure 8, the "Optical Signal Input" is transmitted to the optical divider 6, and the system is "relates to an optical transmission system using RZ (Return to Zero)-modulated signals", it is inherent that an optical transmitter, which transmits the "Optical Signal", is in the system); and

an optical receiver that receives the optical signal transmitted from the optical transmitter, wherein

the optical receiver (Figure 8) includes

an optical divider (Figure 8, the optical divider 8) that divides the received optical signal into a plurality of paths;

a plurality of optical-to-electrical converters (the photoelectric converters 1 in Figure 8) that respectively converts the divided optical input signals into electrical signals;

a plurality of discriminators (the code decision units 3 in Figure 8) that respectively outputs discrimination results by discriminating the electrical signals output from the optical-to-electrical converters based on predetermined thresholds; and

an operational circuit (the OR circuit 5 in Figure 8) that performs a predetermined logical operation with the discrimination results output from the discriminators.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 12-14, 16, 18 and 22 are rejected under 35 U.S.C. 102(a) as being anticipated by Tomizawa et al (US 2003/0118345).

1). With regard to claim 12, Tomizawa et al discloses an optical receiver (e.g., Figures 3-10) comprising:

an optical divider (e.g., the distribution circuit in Figures 3, 8 and 9 etc) that divides an optical input signal into a plurality of paths;

a plurality of optical-to-electrical converters (e.g., the photodetectors in Figures 3, 8 and 9 etc) that respectively converts the divided optical input signals into electrical signals;

a plurality of discriminators (e.g., the decision circuits in Figures 3, 8 and 9 etc) that respectively outputs discrimination results by discriminating the electrical signals output from the optical-to-electrical converters based on predetermined thresholds (the predetermined thresholds: threshold value 1, threshold value 2 etc, or threshold value H, threshold value L etc are used by the discriminators); and

an operational circuit (e.g., the Consensus Logic 4 with the Selection Circuit 5 in Figures 3, 8 and 9 etc) that performs a predetermined logical operation with the discrimination results output from the discriminators ([0045], [0069] and [0070] etc).

2). With regard to claim 13, Tomizawa et al discloses wherein the predetermined thresholds are different from an optimum threshold that is used when discriminating the optical input signals divided into the paths with a single discriminator (Tomizawa et al discloses that the plurality of predetermined thresholds have different values, that is, the predetermined thresholds are different from the single optimum threshold that is used when discriminating the optical input signals divided into the paths with a single discriminator; [0038] and [0039], the thresholds are different from the optimum fixed threshold. Also Tomizawa et al discloses that the threshold value of each decision circuit can be set higher (or lower) than the standard threshold value, [0069]-[0072]).

3). With regard to claim 14, Tomizawa et al discloses wherein

the optical divider is an optical polarization divider (Figure 6, polarization beam splitter can be used to divide the input signal) that divides the optical input signal based on a polarization state of the optical input signal ([0061], “[t]he polarization beam splitter 25 splits optical signals of two polarization modes into each polarization”).

4). With regard to claim 16, Tomizawa et al discloses wherein the predetermined thresholds of the discriminators are substantially equal (e.g., Figure 8, the predetermined thresholds of the discriminators are substantially equal: the threshold value H).

5). With regard to claim 18, Tomizawa et al discloses wherein the operational circuit is a logical OR circuit (e.g., Figure 8 and [0070]-[0072]).

6). With regard to claim 22, Tomizawa et al discloses an optical communication system (e.g., Figures 3-10) comprising:

an optical transmitter (e.g., the optical transmitter shown in Figures 5-7) that transmits an optical signal; and

an optical receiver (e.g., Figures 3-10) that receives the optical signal transmitted from the optical transmitter, wherein

the optical receiver includes

an optical divider (e.g., the distribution circuit in Figures 3, 8 and 9 etc) that divides the received optical signal into a plurality of paths;

a plurality of optical-to-electrical converters (e.g., the photodetectors in Figures 3, 8 and 9 etc) that respectively converts the divided optical imput signals into electrical signals;

a plurality of discriminators (e.g., the decision circuits in Figures 3, 8 and 9 etc) that respectively outputs discrimination results by discriminating the electrical signals output from the optical-to-electrical converters based on predetermined thresholds (the

predetermined thresholds: threshold value 1, threshold value 2 etc, or threshold value H, threshold value L etc are used by the discriminators); and

an operational circuit (e.g., the Consensus Logic 4 with the Selection Circuit 5 in Figures 3, 8 and 9 etc) that performs a predetermined logical operation with the discrimination results output from the discriminators ([0045], [0069] and [0070] etc).

### *Claim Rejections - 35 USC § 103*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomizawa et al (US 2003/0118345) in view of Naito et al (US 5,052,051).

Tomizawa et al disclose all of the subject matter as applied to claims 12 and 14 above, but Tomizawa et al does not expressly disclose an optical polarization controller provided at a pre-stage of the optical polarization divider; a plurality of power monitoring units that respectively monitors optical signal powers on the paths; and a control circuit that controls the optical polarization controller based on the optical signal powers, wherein the control circuit controls the optical polarization controller such that output values of the optical signal powers monitored by the optical monitors become substantially equal.

In Figure 6, Tomizawa et al discloses that a polarization splitter can be used to divide the input signal. However, for a system as shown in Figure 8, or a transmitter as shown in Figures 5 and 7, when a polarization beam splitter is used to divide the input signal, a polarization controller is necessary, otherwise the discriminator and logic circuit cannot properly make the correct decision because of the power difference. Naito et al, teaches a polarization control system, in which an optical polarization controller (e.g., polarization operating apparatus 20 in Figures 2 and 3) provided at a pre-stage of the optical polarization divider (e.g., polarization splitter 23 in Figures 2 and 3); a plurality of power monitoring units (e.g., the receivers 24 and 25 together with the differential amplifier 28; or the power monitors 42 and 43 in Figure 3) that respectively monitors optical signal powers on the paths; and a control circuit (e.g., the polarization control circuit 29 in Figures 2 and 3) that controls the optical polarization controller based on the optical signal powers (e.g., based on the differential signal b from the differential amplifier 28), wherein the control circuit controls the optical polarization controller such that output values of the optical signal powers monitored by the optical monitors become substantially equal (column 3, line 52-56, and column 4 line 53-57, to minimize the signal “b”, that is, output values of the optical signal powers monitored by the optical monitors become substantially equal).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the polarization control mechanism as taught by Naito et al to the system of Tomizawa et al so that the power to the two paths can be substantially equal, and the discriminators can use the substantially same decision

threshold and make a desired decision, and then the system reliability can be increased.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomizawa et al (US 2003/0118345) in view of Sawada et al (WO 03/026239; the corresponding English translation can be found in US 2004/0131368) and Tago et al (US 2004/0165895).

Tomizawa et al disclose all of the subject matter as applied to claim 12 above, and Tomizawa et al also discloses a operational circuit (e.g., Figures 3-6, the Consensus logic and Selection Circuit), to which a plurality of discrimination results from the discriminators is respectively input (e.g., a plurality of discrimination results from the discriminators having different threshold values is respectively input), and a path selecting unit (e.g., Figures 3-6, the Selection Circuit 5) that selects an output result having a low bit error rate based on monitoring information ([0037], [0047], [0056], the output result selected by the Consensus logic and Selection Circuit has a “improved bit error characteristics”).

But Tomizawa et al does not expressly disclose wherein the discriminators are soft decision discriminators, a plurality of operational circuits is provided, to which a plurality of discrimination results from the soft decision discriminators is respectively input, and a bit-error-rate monitoring unit that monitors a bit error rate of an output result of each of the operational circuits; and a path selecting unit that selects an output result having a low bit error rate based on monitoring information of the bit-error-rate monitoring unit.

However, Sawada et al teaches a plurality of soft decision discriminators (e.g., 7 in Figures 3 and 61, or 12 in Figure 4), a probability density distribution estimation circuit (9 in Figures 3 and 61, the probability density distribution estimation circuit is equivalent to the bit error monitoring unit) that monitors the probability density distribution of an output result. And in Figure 14, Sawada et al also discloses a path selecting unit (e.g., selector 23 in Figure 14) that selects outputs based on monitoring information of probability density distribution estimation.

Sawada et al does not expressly state to use the bit error rate for selection. However, another prior art, Tago, teaches bit-error-rate monitoring units (e.g., 46/48 in Figure 8, or 136/138 in Figure 11) that monitor a bit error rate of an output result of each of the discriminators; and then based on monitoring information of the bit-error-rate monitoring units, an optimal decision threshold is determined and used to discriminate the received signals.

But, the combination of Tomizawa et al and Sawada et al and Taga does not expressly disclose a plurality of operational circuits. However, as discussed above, Tomizawa et al teaches a single operational circuit (e.g., Figures 3-6, the Consensus logic and Selection Circuit), and a plurality of discrimination results from a plurality discriminators with different threshold values is respectively input to the single operational circuit. As shown in Figure 3, the set of decision circuit 3-11 to 3-1n has a “threshold value 1”, and the set of decision circuit 3-21 to 3-2n has a “threshold value 2”, and the set of decision circuit 3-k1 to 3-kn has a “threshold value k”; that is, the single Consensus Logic 4 can process k sets of inputs. In applicant's disclosure, as shown in

Figure 7, when a plurality of operational circuits is provided, each operational circuit only receives one set of input which corresponding to a specific decision threshold (Figure 7, e.g., the operational circuit 71-1 receives the results from the discriminators with decision threshold Vth1, and the operational circuit 71-2 receives the results from the discriminators with decision threshold Vth2). Although Tomizawa et al and Sawada et al and Taga do not specifically disclose a plurality of operational circuits (each receives specific discrimination results), such limitation are merely a matter of design choice and would have been obvious in the system of Tomizawa et al and Sawada et al and Taga. The combination of Tomizawa et al and Sawada et al and Taga teaches a plurality of discrimination results from a plurality discriminators with different threshold values is respectively input to the operational circuit, and then a control signal is sent to the selection unit to obtain the desired result. The limitations in claim 17 do not define a patentably distinct invention over that in Tomizawa et al and Sawada et al and Taga since both the invention as a whole and Tomizawa et al and Sawada et al and Taga are directed to select and output the result with improved BER. To use a single operational circuit for all discriminators or use a plurality of operational circuits each responds a specific decision threshold is not critical for the invention as a whole and presents no new or unexpected results, so long as the desire control signal is sent and the result with improved BER is successfully obtained.

Tomizawa et al teaches an operational circuit and path selecting unit to obtained an output with improved bit error rate; and Sawada et al teaches a soft decision discriminator and the information from the probability density distribution can be used to

determine the decision level and also can be used to select the outputs from the soft decision discriminators; and Taga etc teaches to directly use the BER to determine the decision threshold etc. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Sawada et al and Taga to the system of Tomizawa et al so that the bit error rate can be used to control the decision level of the soft decision discriminator and also be used to select the output with low BER, and the selection of the results can be made easier and convenient.

9. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomizawa et al (US 2003/0118345) in view of Hayee et al (US 7,209,671).

Tomizawa et al disclose all of the subject matter as applied to claim 12 above. But, Tomizawa et al does not expressly discloses wherein the operational circuit is a logical AND circuit.

However, Tomizawa et al discloses that the control circuit (consensus logic) can be realized using an OR circuit or an Exclusive OR circuit ([0072]), the threshold values of the discriminators can be higher than the standard threshold or lower than the standard threshold. And another prior art, Hayee et al, discloses an operational circuit (e.g., the Output Decision Circuit in Figure 2, or Figure 5) switches a function of the logical operation based on a control signal (Figure 6, and step 806 in Figure 8; column 7 line 22-64, column 8 line 18-24, and column 9 line 26-36; the output decision circuit applies a selected logic function: OR, AND and XOR).

Hayee et al provide a reliable detection of the received data signal, and the best logic strategy choices can be loaded. Therefore, it would have been obvious to one of

ordinary skill in the art at the time the invention was made to use the logical AND circuit as taught by Hayee et al to the system of Tomizawa et al so that a reliable receiver with improved BER can be obtained.

10. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomizawa et al (US 2003/0118345) in view of Tago et al (US 2004/0165895) and Hayee et al (US 7,209,671).

1). With regard to claim 20, Tomizawa et al disclose all of the subject matter as applied to claim 12 above. But, Tomizawa et al does not expressly discloses a bit-error-rate monitoring unit that monitors a bit error rate of an output result of the operational circuit; and a discrimination-threshold control circuit that changes levels of the predetermined thresholds of the discriminators based on monitoring information of the bit-error-rate monitoring unit, wherein the operational circuit switches a function of the logical operation based on the levels of the predetermined thresholds of the discriminators.

However, Tago et al teaches a bit-error-rate monitoring unit (e.g., 46/48 in Figure 8, or 136/138 in Figure 11) that monitors a bit error rate of output results from one set of discriminators; and a discrimination-threshold control circuit (the Threshold generator in Figure 8, or the Threshold controller 140 in Figure 11) that changes levels of the predetermined thresholds of the discriminator (the Discriminator 40 in Figure 8, or 130 in Figure 11) based on monitoring information of the bit-error-rate monitoring units.

Tago et al teaches a system and method to rapidly determine the best threshold value for the discriminator and stably discriminate a received signal regardless of a time

variation. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Taga to the system of Tomizawa et al so that the bit error rate can be used to control the decision level of the discriminators, and then the receiver can rapidly provide the optimum result.

But, Tago does not expressly discloses the operational circuit switches a function of the logical operation based on the levels of the predetermined thresholds of the discriminators.

However, Tomizawa et al discloses that the control circuit (consensus logic) can be realized using an OR circuit or an Exclusive OR circuit ([0072]), the threshold values of the discriminators can be higher than the standard threshold or lower than the standard threshold. And another prior art, Hayee et al, discloses an operational circuit (e.g., the Output Decision Circuit in Figure 2, or Figure 5) switches a function of the logical operation based on the predetermined thresholds of the discriminators or instruction from a look-up control signal (Figure 6, and step 806 in Figure 8; column 7 line 22-64, column 8 line 18-24, and column 9 line 26-36; the output decision circuit applies a selected logic function: OR, AND and XOR).

By selection of the logical operation, Hayee et al provide a reliable detection of the received data signal, and the best logic strategy choices can be loaded. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the mechanism of selecting the logical operation as taught by Hayee et al to the system of Tomizawa et al and Taga so that the best logic operation can be used

for the specific decision levels of the discriminators, and the reliability of the receiver can be further improved.

2). With regard to claim 21, Tomizawa et al and Taga and Hayee et al disclose all of the subject matter as applied to claim 20 above. And the combination of Tomizawa et al and Taga and Hayee et al further discloses wherein the function of the logical operation includes a logical OR operation and a logical AND operation (Hayee et al: (step 806 in Figure 8; column 8 line 18-24, and column 9 line 26-36; the output decision circuit applies a selected logic function: OR, AND and XOR).

## ***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Moeller (US 2003/0170022);

Moeller et al (US 2005/0185969);

Glingener (US 7,127,166);

Ono (US 5,295,013).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LI LIU whose telephone number is (571)270-1084. The examiner can normally be reached on Monday-Friday, 8:30 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on (571)272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Li Liu/
Examiner, Art Unit 2613
August 27, 2009